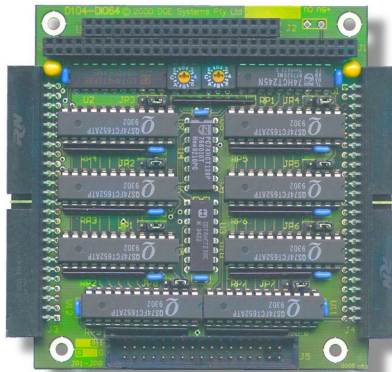


D104-DIO64**64 Line Jumper Programmable Digital I/O Card
for
PC/104 Systems****Rev A**
8th May 2000

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Introduction

The D104-DIO64 provides 64 lines of digital I/O for systems based on the PC/104 format. The digital I/O is configured as eight ports of eight lines with each port individually jumper programmable for input only or for input/output. The ports are labelled PA, PB, PC, PD, PE, PF, PG, PH.

Targeted for industrial applications, the D104-DIO64 is constructed with CMOS logic devices which are rated for operation over an extended temperature range. CMOS components also reduce power requirements.

Features of the D104-DIO64 include:

- **64 lines of jumper programmable I/O**
- **64mA sink/15mA source outputs**
- **OPTO 22 compatible pinouts**
- **Power-up reset**
- **Read back function**
- **PC/104 compliant**
- **CMOS construction**
- **Low power consumption**
- **+5V power supply**

Bus Interface

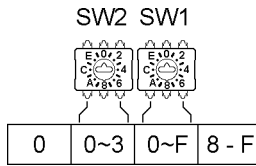
The D104-DIO64 is an I/O mapped, polled, read/write, digital controller occupying 8 contiguous locations in the I/O address space. It interfaces to the PC/104 8-bit bus via connector J1/P1 connector. To maintain 16-bit integrity on the PC/104 stack, the D104-DIO64 is fitted with the J2/P2 stack-through bus connector.

Setting the Base Address

The module's address is set on a 16-byte boundary by two hex-encoded rotary switches. The D104-DIO64 uses offset locations 8 through 15 of this space, it does not respond to offset locations 0 through 7 which are available to other devices.

Users should note that while the I/O address is decoded to 12-bits on the D104-MO32, most PC processors output 10-bit I/O addresses on the system bus. This means addresses 400h and above will not be output by the PC processor limiting the maximum selectable address by SW2 and SW1 to 3F0h.

For the same reason aliasing will occur where the D104-MO32 will respond to a number of different addresses. For example if the base address is set to 330h the module will also be seen at 730h and B30h and FF0h.



Base Address = Address set by SW2, SW1

Address Map		
Base Addr	Function	Access
+0 to +7	No response	Available to other devices
+8	Port PA data	Read/Write
+9	Port PB data	
+A	Port PC data	
+B	Port PD data	
+C	Port PE data	
+D	Port PF data	
+E	Port PG data	
+F	Port PH data	

Table 1: Address Map

I/O Structure

The following diagram is useful for understanding the I/O structure for each port. All ports on the D104-DIO64 are permanently enabled for reading. Each input line is terminated with a pull-down resistor to logic low, ensuring a known logic state for unconnected inputs.

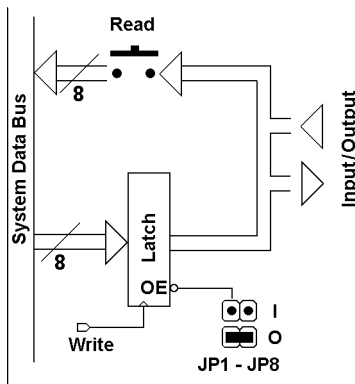


Figure 2: I/O Structure Diagram

Output Mode

When a port is enabled for output, the digital output line is able to sink 64mA at logic low and source 15mA at logic high. Users should be realistic in their expectations as to the amount of output signal drive, sixty four lines each sinking 64mA may well exceed the capability of the D104-DIO64 or the system power supply to provide over 4 amps!

Since a port's input stage is always enabled, readback of the output data is possible. This feature is useful for retrieving (or confirming) output values. The output data latch can be written to even if output enable is not set.

Jumper links JP1 to JP8 must be set to enable/disable output mode.

Jumper Links	
Port	Use Jumper
Port PA data	JP1
Port PB data	JP2
Port PC data	JP3
Port PD data	JP4
Port PE data	JP5
Port PF data	JP6
Port PG data	JP7
Port PH data	JP8

Table 2: JP1 to JP8 Links

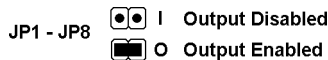


Figure 3: JP1 to JP8 Link Settings

A limited, software-programmable feature is possible on the D104-DIO64. This is achieved by assigning (say) port PH for output and connecting its output pins to pin 2 of jumpers 1 through 7.

The output enable for ports PA to PG inclusive, can then be programmed by setting the appropriate bits in port PH,

Reset

The D104-DIO64 output latches are set to logic low on power up. Systems builders will appreciate the importance of having the D104-DIO64 power up in a known "all outputs off" state.

The module however, does not respond to a system reset or warm boot. The state of the outputs will be maintained.

Industry Standard Pinouts

The I/O is in accordance with "OPTO 22" pin mapping. This allows the D104-DIO64 to interface to popular solid-state module racks for the optically-isolated sensing of, and the optically-isolated switching of DC and AC voltages.

D104 Series Buffer Modules

The D104-DIO64 is compatible with the D104 series of buffer modules. These have a PC/104 formfactor and can be bolted onto the PC/104 stack. All modules have two-part detachable terminal blocks for easy connect/disconnect of field wiring.

The series consists of:-

D104-IM24	24 lines of optically isolated inputs
D104-RM24P	24 SPST relay outputs, 5A/250Vac
D104-MM816	8 SPST relay out, 24 opto-isolated inputs
D104-OM24	24 opto-isolated MOSFET SSRs, AC/DC switching

Connector Pin Assignments

Connector J1/P1 Pin Assignments			
Signal	Pin	Pin	Signal

/IOCHCHK		1a	1b	□	0V (Gnd)
SD7	□	2a	2b	□	RESETDRV
SD6	□	3a	3b	□	+5V (VCC)
SD5	□	4a	4b		IRQ2/9
SD4	□	5a	5b		-5V
SD3	□	6a	6b		DRQ2
SD2	□	7a	7b		-12V
SD1	□	8a	8b		/ENDXFR
SD0	□	9a	9b		+12V
IOCHRDY		10a	10b		(KEY)
AEN	□	11a	11b		/SMEMW
SA19		12a	12b		/SMEMR
SA18		13a	13b	□	/IOW
SA17		14a	14b	□	/IOR
SA16		15a	15b		/DACK3
SA15		16a	16b		DRQ3
SA14		17a	17b		/DACK1
SA13		18a	18b		DRQ1
SA12		19a	19b		/REFRESH
SA11	□	20a	20b		CLK
SA10	□	21a	21b		IRQ7
SA9	□	22a	22b		IRQ6
SA8	□	23a	23b		IRQ5
SA7	□	24a	24b		IRQ4
SA6	□	25a	25b		IRQ3
SA5	□	26a	26b		/DACK2
SA4	□	27a	27b		TC
SA3	□	28a	28b		BALE
SA2	□	29a	29b	□	+5V
SA1	□	30a	30b		OSC
SA0	□	31a	31b	□	0V (Gnd)
0V (Gnd)	□	32a	32b	□	0V (Gnd)

Connector J2/P2 Pin Assignments			
Signal	Pin	Pin	Signal

0V (Gnd)		0c	0d		0V (Gnd)
/SBHE		1c	1d		/MEMCS16
LA23		2c	2d		/IOCS16
LA22		3c	3d		IRQ10
LA21		4c	4d		IRQ11
LA20		5c	5d		IRQ12
LA19		6c	6d		IRQ15
LA18		7c	7d		IRQ14
LA17		8c	8d		/DACK0
/MEMR		9c	9d		DRQ0
/MEMW		10c	10d		/DACK5
SD8		11c	11d		DRQ5
SD9		12c	12d		/DACK6
SD10		13c	13d		DRQ6
SD11		14c	14d		/DACK7
SD12		15c	15d		DRQ7
SD13		16c	16d		+5V (VCC)
SD14		17c	17d		/MASTER
SD15		18c	18d		0V (Gnd)
(KEY)		19c	19d		0V (Gnd)

□ Signals used on the D104-DIO64

Table 3: Connector J1/P1 and J2/P2 Pin Assignments

J3 Connector Pin Assignments					J4 Connector Pin Assignments							
Base	Bit	Signal	Pin	Pin	Signal	Base	Bit	Signal	Pin	Pin	Signal	
+8	7	PA7	1	2	Gnd	+B	7	PD7	1	2	Gnd	
	6	PA6	3	4			6	6	PD6	3		4
	5	PA5	5	6			8	5	PD5	5		6
	4	PA4	7	8			10	4	PD4	7		8
	3	PA3	9	10			12	3	PD3	9		10
	2	PA2	11	12			14	2	PD2	11		12
	1	PA1	13	14			16	1	PD1	13		14
	0	PA0	15	16			18	0	PD0	15		16
+9	7	PB7	17	18		+C	7	PE7	17	18		
	6	PB6	19	20			6	PE6	19	20		
	5	PB5	21	22			5	PE5	21	22		
	4	PB4	23	24			4	PE4	23	24		
	3	PB3	25	26			3	PE3	25	26		
	2	PB2	27	28			2	PE2	27	28		
	1	PB1	29	30			1	PE1	29	30		
	0	PB0	31	32			0	PE0	31	32		
+A	7	PC7	33	34		+D	7	PF7	33	34		
	6	PC6	35	36			6	PF6	35	36		
	5	PC5	37	38			5	PF5	37	38		
	4	PC4	39	40			4	PF4	39	40		
	3	PC3	41	42			3	PF3	41	42		
	2	PC2	43	44			2	PF2	43	44		
	1	PC1	45	46			1	PF1	45	46		
	0	PC0	47	48			0	PF0	47	48		
+5V			49	50		+5V			49	50		

Table 4: J3 and J4 Pin Assignments

J5 Connector Pin Assignments					
Base	Bit	Signal	Pin	Pin	Signal
+E	0	PG0	1	2	Gnd
	1	PG1	3	4	
	2	PG2	5	6	
	3	PG3	7	8	
	4	PG4	9	10	
	5	PG5	11	12	
	6	PG6	13	14	
	7	PG7	15	16	
+F	0	PH0	17	18	
	1	PH1	19	20	
	2	PH2	21	22	
	3	PH3	23	24	
	4	PH4	25	26	
	5	PH5	27	28	
	6	PH6	29	30	
	7	PH7	31	32	
+5V			33	34	

Table 5: J5 Pin Assignments

Component Layout

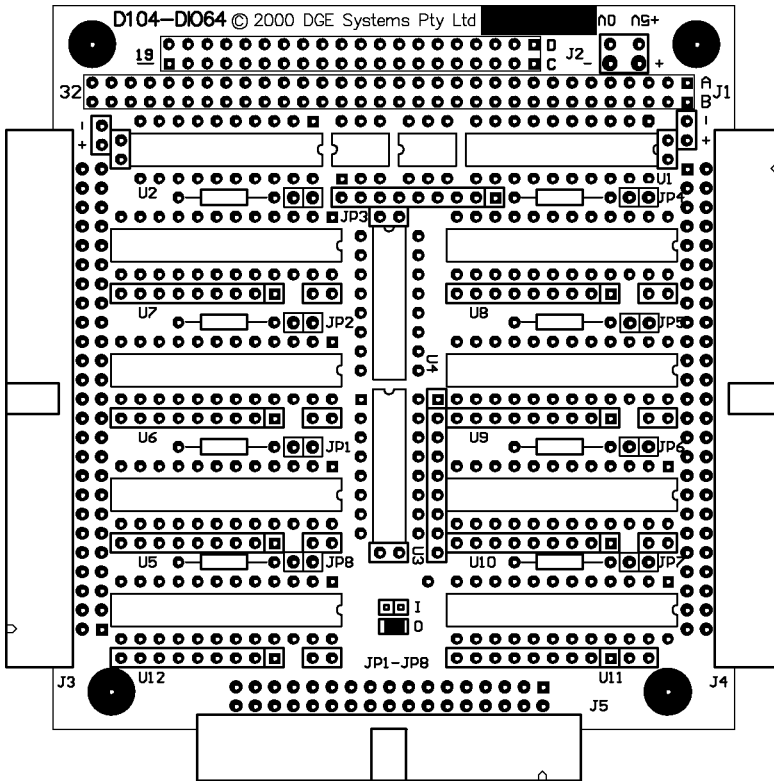


Figure 4: Component Layout

Specifications

Specifications	
Bus Interface:	8 bit, PC/104 compliant.
I/O Space:	Occupies 8 I/O locations within 16 byte boundary. at offsets +8 to +F
Output Sink: Source:	64mA, 0.55V max (VOL) 15ma, 2.4V min (VOH)
Input Low: High:	0.8V max, 5 µA typical 2.0V min, 5 µA typical
Connectors Bus: I/O:	J1/P1, J2/P2 (stackthrough) 2 x 50 pin IDC (J3, J4), 1 x 34 pin IDC (J5)
Power Requirements:	+5Vdc
Temperature: Operating: Storage:	-20 to +70°C. * -55 to +100°C.
Humidity:	5% to 95% non condensing.
Dimensions:	90 x 96mm (3.55 x 3.775")
Weight:	xxg approx.

** Absolute Maximum Rating in free air. Caution is advised when extended temperature operation is considered. Thermal management strategies must ensure semiconductor components are not exposed to conditions beyond their capability. Product reliability may be compromised.*

Ordering Information

Order Code	Output Rating
D104-DIO64	PC/104 64 Line I/O Module
D104-DIO64-TM	Technical Manual