

CM-388 Technical Manual

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packing list

Hardware

CM-388 PC/104 Module x 1

Cables

IDE flat cable x 1

Floppy Drive flat cable x 1

Dual Port RS-232 cable with bracket (9/25 pin) x 1

Printer Port cable with bracket x 1

5-pin header to keyboard converter cable x 1

10-pin header to 15-pin D-type VGA converter cable x 1

10-pin header to 9-pin D-type RS-232 converter cable x 1

PC/104 screw package x 1

Printed Matter

CM-388 User's Manual x 1

Warranty Card x 1

Software

CM-388 Driver & Utilities Disk (3½", 1.44MB) x 1

Introduction

The CM-388 contains all standard motherboard features such as : 386SX-40 compatible CPU, 4 MB DRAM onboard, CRT and Flat Panel SVGA controller, serial and parallel ports, floppy and EIDE disk controller.

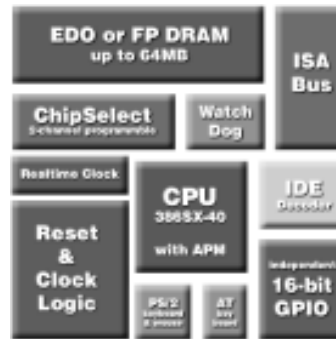
The modules SSD socket can accommodate a DiskOnChip®2000, a new generation of high performance single-chip Flash Disks of up to 144 MB.

The CM-388 is a core module for high performance control applications in demanding embedded applications. Because the module implements all key functions of a full PC/AT compatible system any standard PC compiler or debugger can be used, resulting in a significantly reduced software development cycle.

M6117D

A highly integrated embedded solution

386SX-40 Core, 16-bit independent GPIO connects directly to ASCII Display, 2-channel Programmable Chip Select, EDO and FP DRAM up to 64 MB, Realtime Clock, Watch-dog Timer, ISA Interface, PS2 Keyboard/Mouse Controller, Peripheral Interface with DMA Controller, IDE Interface, PMU Interface, Memory Mapper, Interrupt Controller and Program Counter. (Check in the specifications which functions are actually enabled for different products)



Application Development

The best thing about using PC compatible hardware is that ready availability of a large amount of low priced development tools. Development platforms like Assembly, C, Pascal, Basic are mainstream and come with a great source of programming examples.

Operating System

An Intel compatible 386SX core leaves you in charge to decide what operating system you will use. Choose from a variety of systems ranging from rock solid operating systems like Caldera's Embedded DOS to Realtime QNX.

Specifications

- **CPU + Chipset** : ALI M6117D is an implementation of an INTEL compatible 386SX-40 CPU, Realtime clock, a watchdog timer and ALI's M1217B chipset
- **BIOS** : Y2K compliant AMI system BIOS
- **DRAM Memory**: 4MB EDO DRAM onboard
- **Bus Interface** : PC/104
- **Data Bus** : 16-bit
- **Bus Speeds** : PC/104 - 8 MHz
(above values are defaults, bus speeds are programmable up to 16 MHz)
- **DMA Controllers** : 8237 x 2
- **DMA Channels** : 7
- **Interrupt Controllers** : 8259 x 2
- **Interrupt Levels** : 15
- **Enhanced IDE** : supports one port and up to two hard drives or Enhanced IDE devices of PIO mode 4. BIOS enabled/disabled
- **Watchdog Timer** : generates either a RESET, NMI or an IRQ when your application loses control over the system. Optionally the watchdog can trigger a user specified interrupt. The watchdog is configurable from 30.5 μ s to 512 seconds (in 30.5 μ s segments)
- **Real-time Clock** : included in M6117D with onboard lithium battery backup for 10 years of data retention. CMOS data backup of BIOS setup and BIOS default.
- **Keyboard and Mouse Connectors**:
Internal 5-pin header for AT-keyboard
Internal 5-pin header for PS/2-mouse

High Speed Multi I/O

- **Chipset** : ALI 5113
- **Serial ports**: one high speed RS-232 port, one high speed RS-232/485 port (jumper selectable). Both with 16C550 UART and 16 byte FIFO. BIOS enabled/disabled
- **Floppy Disk Drive Interface**: supports up to two floppy drives, 5¼ " (360 KB or 1.2 MB) and 3½ " (720 KB, 1.44 MB). BIOS enabled/disabled
- **Bi-directional Parallel Port** : supports SPP, EPP and ECP mode. BIOS enabled/disabled

Flat Panel Display Controller

- **Chipset** : HMC HM86508
- **Memory** : 1 MB onboard
- **System Bus** : 16-bit ISA bus
- **Panel Data Bus** : 24-bit
- **Display** : CRT and Flat Panel Mono/TFT/DSTN/EL
- **Supported Flat Panels** :

NEC	NL-6448AC30-10	TFT 9.4" 640X480
NEC	NL-6448AC30-03	TFT 9.4" 640X480
NEC	NL-6448AC33-10	TFT 10.4" 640X480
NEC	NL-6448AC33-13	TFT 10.4" 640X480
NEC	NL-6448AC33-18	TFT 10.4" 640X480
NEC	NL-8060BC31-09	TFT 12.1" 800X600
NEC	NL-8060AC31-02	TFT 10.4" 800X600
NEC	NL-8060AC31-01	TFT 10.4" 800X600
SHARP	LQ10D42	TFT 10.4" 640X480
SHARP	LQ10D421	TFT 10.4" 640X480
SHARP	LQ12531	TFT 12.1" 800x600
SHARP	LM64C35P	MONO 10.4" 640X480
Planar	EL640.480-AA1	EL color 10.4" 640X480

Check for other displays.

- **Compatibility** : IBM VGA hardware

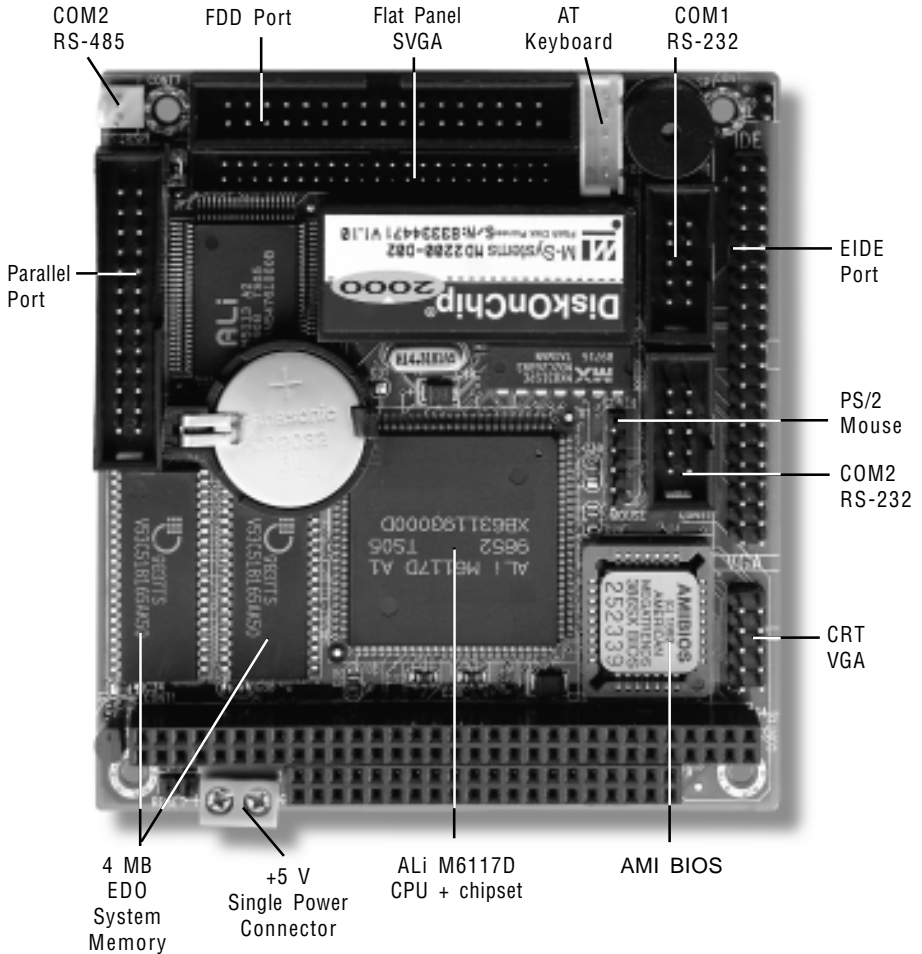
Flash Disk DiskOnChip®2000

- **Package** : Single Chip FlashDisk in 32-pin DIP JEDEC
- **Capacity** : 1-144 MByte capacity
- **Data Reliability** : ECC/EDC error correction
- **Memory Window** : 8 KByte

Environmental and Power

- **Power Requirements**:
single voltage +5 V @ 800 mA with 4 MB EDO installed
- **Board Dimensions** : 90 (L) x 96 (W) mm.
- **Board Weight** : 105 g
- **Extended Operating Temperature**: -20~+60 °C

Component Location

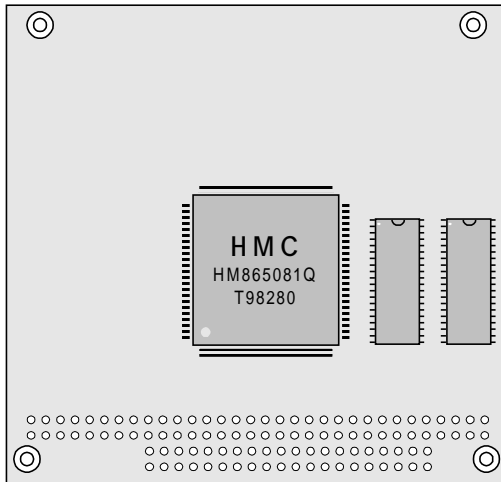
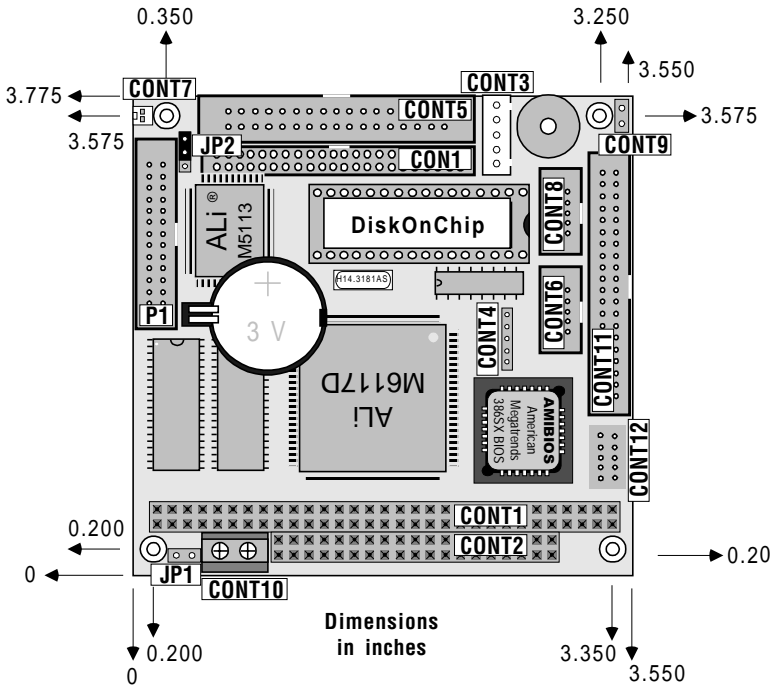


Warning

PC/104 Modules and their components contain very delicate Integrated Circuits (IC). To protect the PC/104 Module and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your PC/104 Module from the power source whenever you want to handle the module
2. Use a grounded wrist strap when handling the module.
3. Hold the module by the edges and try not to touch the IC chips, leads or circuitry
4. Place the module on a grounded antistatic pad or on the bag that came with the PC/104 Module when handling it.

Board Layout



Jumper/Connector Quick Reference

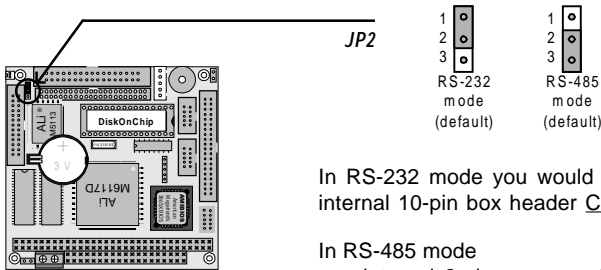
JP1	RESET connector
JP2	RS-232/485 selection for COM2 1-2 -> RS-232 mode (CONT6 active) 2-3 -> RS-485 mode (CONT7 active)
CON1	Internal 44-pin Flat Panel SVGA connector
CONT1	PC/104 bus 64-pin
CONT2	PC/104 bus 40-pin
CONT3	AT-keyboard connector
CONT4	PS/2 Mouse
CONT5	FDD controller
CONT6	COM2 RS-232
CONT7	COM2 RS-485
CONT8	COM1 RS-232
CONT9	IDE LED
CONT10	Power Connector
CONT11	IDE connector
CONT12	CRT SVGA connector
P1	Parallel Port

Jumper Settings

The CM-388 has an AMI BIOS. Most settings for peripherals such as COM ports, HDD, FDD and printer port are done in the BIOS setup. However some settings are done by jumpers

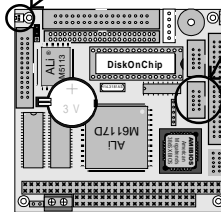
COM2 RS-232/485 selection (JP2)

The CM-388 offers two serial ports: one RS-232 and one RS232/485. These ports let you connect to serial devices (mouse, printers, etc.), or to a communication network. The CM-388 serial ports can be configured in the BIOS. COM2 uses a different connector for RS-232 (CONT6) and RS-485 (CONT7) mode. You can select this mode with JP2.



In RS-232 mode you would connect to internal 10-pin box header CONT6

In RS-485 mode use internal 2-pin header CONT7



DiskOnChip® 2000 Flash Disk

Installation Instructions

1. Make sure the CM-388 is powered OFF
2. Plug the DiskOnChip 2000 device(s) into its socket. Verify the direction is correct (pin 1 of the DiskOnChip 2000 is aligned with pin 1 of the socket)
3. Power up the system
4. Go to BIOS Setup's "Advanced Chipset Setup"

5. The GPCS (General Purpose Chip Select) function is used to enable/disable the DiskOnChip function. (see also page 36-38)

GPCS Function	Enable
GPCS0 Command	MEMR/W 8bit
GPCS0 Start Address	0C8000 Hex
GPCS0 Size	8 KBYTE

- GPCS0 Command = always MEMR/W 8bit
- GPCS0 Start Address = configurable between C8000h DE000h
- GPCS0 Size = always 8 KBYTE

Save the settings and reboot the computer.

4. During power up you may observe the messages displayed by the DiskOnChip 2000 when its drivers are loaded into system's memory
5. At this stage the DiskOnChip 2000 can be accessed as any disk in the system
6. If the DiskOnChip 2000 is the only disk in the system, it will appear as the first disk (drive C: in DOS)
7. If there are more disks besides the DiskOnChip 2000, the DiskOnChip 2000 will appear by default as the last drive, unless it was programmed as first drive. (please refer to the DiskOnChip 2000 utilities user manual)
8. If you want the DiskOnChip 2000 to be bootable:
 - a - copy the operating system files into the DiskOnChip by using the standard DOS command (for example: sys d:)
 - b - The DiskOnChip should be the only disk in the systems or should be configured as the first disk in the system (c:) using the DUPDATE utility

For more information on DiskOnChip2000 technology, visit M-Systems Web site

[http:// www.m-sys.com](http://www.m-sys.com)

where you can find Utilities Manual, Data Sheets and Application Notes. In addition, you can find the latest DiskOnChip 2000 S/W Utilities

Watchdog Timer

The watchdog timer uses a 32.768 KHz frequency source with a 24-bit counter. Its time range stretches from 30.5 μ s to 512 sec. with a resolution of 30.5 μ s. When the watchdog times out a System RESET, NMI or IRQ can be invoked. Watchdog timer control and the 24-bit counter itself occupy 6 consecutive 8-bit address locations.

When functioning properly the system resets the watchdog timer periodically to prohibit that it times out. If the watchdog timer times out, it will RESET the system, or generate and NMI or IRQ, depending on its configuration.

Watchdog or System Timer

Another great application is to generate a periodic IRQ signal. Under DOS environment, the 8254, system timer 0, will generate IRQ0 every 54.9 ms. The watchdog is like system timer 0. It can be programmed to periodically generate a configurable IRQ. It may be clear that the selected IRQ, will be no longer available to the system.

Configuring the Watchdog Timer in the BIOS

The M6117D watchdog configuration register can be controlled by software or can be setup in the BIOS. To do so go to BIOS Setup's "Advanced Chipset Setup" (see also pages 36-38)

Watchdog Function	Enable
Watchdog Signal	Reset
Watchdog Timer	64 Sec

- Watchdog Function = Enable/Disable
- Watchdog Signal = RESET, NMI or IRQ 3/4/5/6/7/9/10/11/12/14/15
- Watchdog Timer = 1/2/4/8/16/32/64/128/256/512 Seconds

The BIOS setup only offers a limited amount of time-out values. More a higher resolution of timeout values refer to the next paragraph "Configuring the Watchdog Timer by Software"

Note that in case of using the BIOS setup, the watchdog starts counting the moment it passes the BIOS setup. This means that if you set the time-out period to 1 second, the system will keep rebooting before being able to load operating system or software !

After you have finished configuring your watchdog timer read "Timeout Status & Reset - INDEX 3CH" on page 12 and look at the example on page 15 to find out how to periodically reset the timeout status to prevent the watchdog timer from invoking a RESET, NMI or IRQ.

Configuring the Watchdog Timer by Software

Chipset configuration registers

The M6117D configuration register INDEX 37H, 38H, 39H, 3AH, 3BH, 3Ch are used to control the watchdog functions and/or display its current status.

Enable/Disable watchdog - INDEX 37H

Bit	Value	Action
7	reserved.	Do not modify the value of this bit !
6	0	disable watchdog timer
	1	enable watchdog timer
5~0	Other function	Do not modify the value of these bits !

Watchdog time out action - INDEX 38H

Bit	Value	Action
7~4	0000	no output signal
	0001	IRQ3
	0010	IRQ4
	0011	IRQ5
	0100	IRQ6
	0101	IRQ7
	0110	IRQ9
	0111	IRQ10
	1000	IRQ11
	1001	IRQ12
	1010	IRQ14
	1011	IRQ15
	1100	NMI
	1101	system RESET
	1110	no output signal
	1111	no output signal
3-0	other function, do not modify these bits !	

Watchdog timer - INDEX 39H, 3AH, 3BH

Index	3Bh	3Ah	39h
Bits	D7.....D0	D7.....D0	D7.....D0
counter	[MSB.....LSB]		

for example,

INDEX	3Bh	3Ah	39h	time out
	00h	00h	01h	30.5 μ sec
	00h	00h	02h	61 μ sec
	00h	01h	00h	7.8 msec
	00h	02h	00h	15.6 msec
	01h	00h	00h	2 sec
	02h	00h	00h	4 sec
	FFh	FFh	FFh	512 sec

Timeout Status & Reset - INDEX 3CH

Bit	Value	Action	remarks
7	0	timeout has not (yet) occurred	read only
	1	timeout has occurred	
6			
5	write 1	reset timer	
	0	has no meaning	
4-0	other function, do not modify these bits !		

Programming the watchdog

To perform any operation on the M6117D configuration registers you always have to unlock first and lock the registers afterwards

Unlock configuration register

```
mov    al, 013h
out    22h, al
nop
nop
mov    al, 0c5h
out    23h, al
nop
nop
```

Lock configuration register

```
mov    al, 013h
out    22h, al
nop
nop
mov    al, 000h
out    23h, al
nop
nop
```

Read the value of a configuration register

For example, read INDEX 3Ch :

Unlock configuration register

```
mov    al, 03ch
out    22h, al
nop
nop
in     al, 23h
nop
nop
push   ax
```

Lock configuration register

```
pop    ax      ; AL - result
```

Write data to configuration register

For example, write 0FFh to INDEX 3Bh :

Unlock configuration register

```
mov    al, 03bh
out    22h, al
nop
nop
mov    al, 0ffh
out    23h, al
nop
nop
```

Lock configuration register

Watchdog Program Example

We use the following sequence to initialize the watchdog timer:

- (1) Unlock configuration register.
- (2) Disable watchdog timer by setting INDEX 37H Bit 6 to '0'.
- (3) Set the expected counter value to INDEX 3BH, 3AH, 39H.
- (4) Select timeout action from INDEX 38H Bit 7-4.
- (5) Enable watchdog timer by setting INDEX 37H Bit 6 to '1'.
- (6) Lock configuration register.

Example: Set timeout to 128 sec to generate a system RESET.

```
; Please use MASM to compiler the following program
; Execute under DOS environment
dosseg
. model small
. stack      100h
.code
main proc
    mov     ax, 0c513h    ; Unlock config. register
    call   writechip
    mov     ax, 03737h    ; Disable watchdog timer
    call   readchip
    and     al, 10111111b
    xchg   ah, al
    call   writechip
    mov     ax, 0403bh    ; Set the expected counter
                        ; value
    call   writechip     ; to [400000h]
    mov     ax, 0003ah    ; 30.5*sec*400000h= 128 sec
    call   writechip
    mov     ax, 00039h
    call   writechip
    mov     ax, 03838h    ; Select "system reset" as
                        ; timeout action

    call   readchip
    and     al, 00001111b
    or      al, 11010000b
    xchg   ah, al
    call   writechip

    mov     ax, 03737h    ; Enable watchdog timer
    call   readchip
    or      al, 01000000b
    xchg   ah, al
    call   writechip

    mov     ax, 00013h    ; Lock config. register
    call   writechip
    mov     ax, 04c00h
    int     21h

main endp
```

```

readchip proc
    out        22h, al
    nop
    nop
    in         al, 23h
    nop
    nop
    ret
readchip endp

writechip proc
    out        22h, al
    nop
    nop
    xchg       ah, al
    out        23h, al
    nop
    nop
    xchg       ah, al
    ret
writechip endp

end main

```

Reset watchdog timer

Resets the watchdog timer periodically to prevent timeout.

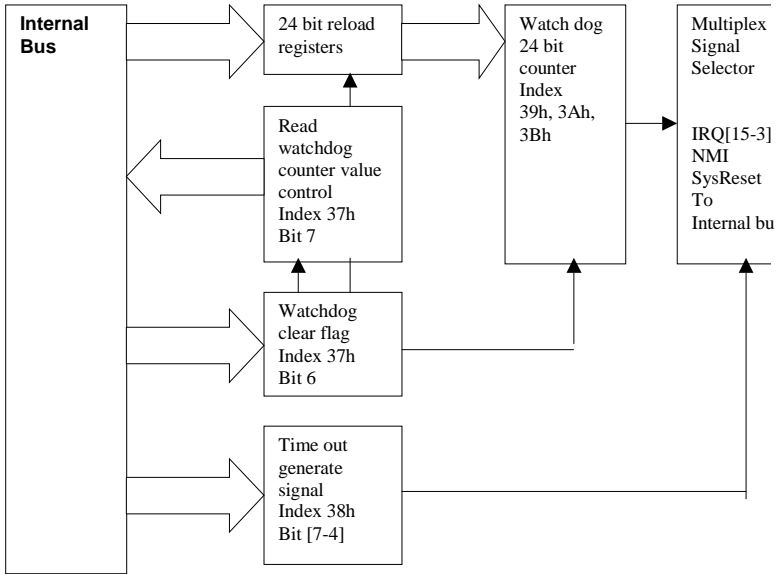
```

mov    ax, 0c513h    ; Unlock configuration
                        ; register
call   writechip
mov    ax, 03C3Ch    ; Reset watchdog timer
                        ; counter
call   readchip
or     al, 00100000b ; The counter is reset at
xchg   ah, al        ; out 23h, al
call   writechip
mov    ax, 00013h    ; Lock configuration
                        ; register
call   writechip

```

(the above code uses *readchip* and *writechip* procedures)

Watchdog Timer Block Diagram

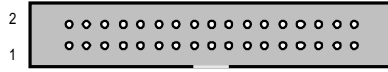


Interface Connectors HDD, FDD

Floppy Disk Drive (CONT5)

Connector : **CONT5**

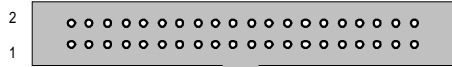
Type : Onboard 34-pin header



CONT5

Pin	Description	Pin	Description
1	GROUND	2	REDUCE WRITE
3	GROUND	4	N/C
5	GROUND	6	N/C
7	GROUND	8	INDEX#
9	GROUND	10	MOTOR ENABLE A#
11	GROUND	12	DRIVE SELECT B#
13	GROUND	14	DRIVE SELECT A#
15	GROUND	16	MOTOR ENABLE B#
17	GROUND	18	DIRECTION#
19	GROUND	20	STEP#
21	GROUND	22	WRITE DATA#
23	GROUND	24	WRITE DATA#
25	GROUND	26	TRACK 0#
27	GROUND	28	WRITE PROTECT#
29	GROUND	30	READ DATA#
31	GROUND	32	SIDE 1 SELECT
33	GROUND	34	DISK CHANGE#

Enhanced IDE Connector (CONT11)



CONT11

Connector : **CONT11**

Type : onboard 40-pin header, primary IDE

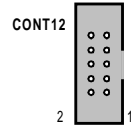
Pin	Description	Pin	Description
1	RESET	2	GROUND
3	DATA 7	4	DATA 8
5	DATA 6	6	DATA 9
7	DATA 5	8	DATA 10
9	DATA 4	10	DATA 11
11	DATA 3	12	DATA 12
13	DATA 2	14	DATA 13
15	DATA 1	16	DATA 14
17	DATA 0	18	DATA 15
19	GROUND	20	N/C
21	N/C	22	GROUND
23	IOW#	24	GROUND
25	IOR#	26	GROUND
27	N/C	28	BALE - DEFAULT
29	N/C	30	GROUND# -DEFAULT
31	INTERRUPT	32	IOCS16#-DEFAULT
33	SA1	34	N/C
35	SA0	36	SA2
37	HDC CS0	38	HDC CS1#
39	HDD ACTIVE	40	GROUND

Peripheral Ports

CRT SVGA (CONT12)

Connector : **CONT12**

Type : internal 10-pin box header

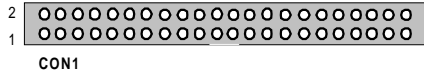


Pin	Description	Pin	Description
1	RED	2	GND
3	GREEN	4	GND
5	BLUE	6	GND
7	HSYNC	8	GND
9	VSYNC	10	GND

Flat Panel VGA (CON1)

Connector : **CON1**

Type : Onboard 44-pin header

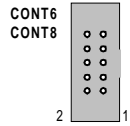


Pin	Description	Pin	Description
1	+12	2	+12
3	GND	4	GND
5	PVcc	6	PVcc
7	FPVee	8	GND
9	PD0	10	PD1
11	PD2	12	PD3
13	PD4	14	PD5
15	PD6	16	PD7
17	PD8	18	PD9
19	PD10	20	PD11
21	PD12	22	PD13
23	PD14	24	PD15
25	PD16	26	PD17
27	PD18	28	PD19
29	PD20	30	PD21
31	PD22	32	PD23
33	GND	34	GND
35	SHFCLK	36	FLM
37	M	38	LP
39	GND	40	ENABKL
41	GND	42	ASHFCLK
43	VCC	44	VCC

External RS-232 Serial Port (CONT6, CONT8)

Connector : **CONT6 & CONT8**

Type : onboard 10-pin box header



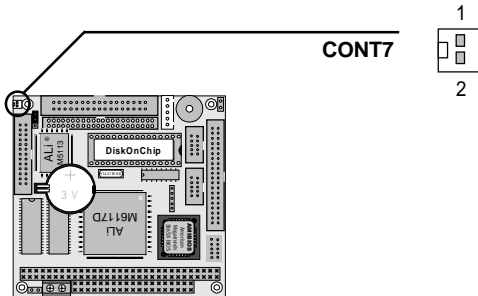
Pin	Description	Pin	Description
1	DCD	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI	10	NC

Internal RS-485 Serial Port (CONT7)

Connector : **CONT7**

Type : onboard 2-pin header (COM2)

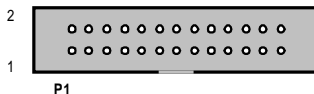
Pin	Description
1	RS-485+
2	RS-485-



Parallel Port (P1)

Connector : **P1**

Type : onboard 26-pin box header

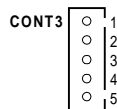


Pin	Description	Pin	Description
1	STROBE	2	DATA 0
3	DATA 1	4	DATA 2
5	DATA 3	6	DATA 4
7	DATA 5	8	DATA 6
9	DATA 7	10	ACKNOWLEDGE
11	BUSY	12	PAPER EMPTY
13	PRINTER SELECT	14	AUTO FORM FEED
15	ERROR#	16	INITIALIZE
17	PRINTER SELECT LN#	18	GROUND
19	GROUND	20	GROUND
21	GROUND	22	GROUND
23	GROUND	24	GROUND
25	GROUND	26	NC

AT Keyboard (CONT3)

Connector : **CONT3**

Type : Onboard 5-pin header

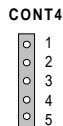


Pin	Description	Pin	Description
1	KEYBOARD CLOCK	2	KEYBOARD DATA
3	N/C	4	GROUND
5	+5V		

PS/2 Mouse (CONT4)

Connector : **CONT4**

Type : onboard 5-pin header

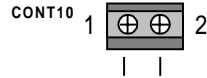


Pin	Description	Pin	Description
1	MCLK	2	IRQ12
3	NC	4	GND
5	Vcc		

Power Connector (CONT10)

Connector : **CONT10**

Type : dual screw block terminal

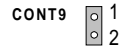


Pin	Description
1	Vcc (+)
2	GND (-)

IDE LED (CONT9)

Connector : **CONT9**

Type : 2-pin header



Pin	Description
1	Vcc (+)
2	IDE LED (-)

Flat Panel BIOS and Wiring

Below is a list of optional Flat Panel SVGA BIOS. The VGA BIOS is combined with the system BIOS in a single image. To change to another BIOS please contact your local dealer.

MLCD.dat - Data File for MONO DSTN640*480 (Default)

example : (1) HOSIDEN HLM6667
(2) HITACHI LMG5160XUFC
(3) CASIO MD650TS00-01
(4) OPTREX DMF_50260NFU-FW-8

DSTN.dat - Data file for Color DSTN640*480

example : (1) Sanyo LCM-5331-22NTK
(2) SHARP LM64C35P

TFT_S1.dat - Data File for TFT640*480-Sync (16 BIT)

TFT_S2.dat - Data File for TFT640*480-Sync (18/24 BIT)

example : (1) HITACHI TX26D60/TX24D55
(2) TOSHIBA LTM09C015A
(3) SHARP LQ10D321

TFT_LP1.dat - Data File For TFT640*480-LP (16 BIT)

TFT_LP2.dat - Data File For TFT640*480-LP (18/24 BIT)

example : (1) Toshiba LTM09c015A)

TFT86_S1.dat - Data File for TFT800*600_sync (16 BIT)

TFT86_S2.dat Data File for TFT800*600_sync (18/24 BIT)

example : (1) NEC NL8060AC26-05
(2) NEC NL8060AC26-04
(3) NEC NL8060BC31-02

EL.dat - Data File for EL640*480

example : (1) PLANAR EL640.480-A

PLASMA.dat - Data File for PLASMA640*480

example : (1) PANASONIC S817

CRT/Flat Panel Mode

All the above BIOS support either CRT only, Flat Panel only or CRT/Flat Panel simultaneously. To set the mode a Panel Switching Utility is used.

USAGE:

At DOS prompt type >SW508 then Screen will show

1. CRT Only
2. Panel Only
3. CRT/Panel Simutaneous

NEC NL6448AC33-18 wiring

NEC NL6448AC33-18		PIA-3386DV CON1	
Pin	Pin name	Pin	Pin name
CN1-1	GND	3	GND
CN1-2	CLK	35	SHFCLK
CN1-3	Hsync	38	LP
CN1-4	Vsync	36	FLM
CN1-5	GND	4	-
CN1-6	R0	27	P18
CN1-7	R1	28	P19
CN1-8	R2	29	P20
CN1-9	R3	30	P21
CN1-10	R4	31	P22
CN1-11	R5	32	P23
CN1-12	GND	33	-
CN1-13	G0	19	P10
CN1-14	G1	20	P11
CN1-15	G2	21	P12
CN1-16	G3	22	P13
CN1-17	G4	23	P14
CN1-18	G5	24	P15
CN1-19	GND	34	-
CN1-20	B0	11	P2
CN1-21	B1	12	P3
CN1-22	B2	13	P4
CN1-23	B3	14	P5
CN1-24	B4	15	P6
CN1-25	B5	16	P7
CN1-26	GND	39	-
CN1-27	ENAB	37	MDE
CN1-28	Vcc	43	Vcc
CN1-29	Vcc	44	Vcc
CN1-30	NC	-	-
CN1-31	NC	-	-

NEC NL6448AC30-10 wiring

(800 x 600 TFT Color)

NEC NL6448AC30-10		PIA-3386DV CON1	
Pin	Pin name	Pin	Pin name
CN1-1	CLK	42	SHFCLK
CN1-2	Hsync	38	LP
CN1-3	Vsync	36	FLM
CN1-4	DE	37	MDE
CN1-5	-	-	P0
CN1-6	B0	10	P1
CN1-7	B1	11	P2
CN1-8	B2	12	P3
CN1-9	B3	13	P4
CN1-10	-	14	P5
CN1-11	-	15	P6
CN1-12	G0	16	P7
CN1-13	G1	17	P8
CN1-14	G2	18	P9
CN1-15	G3	19	P10
CN1-16	-	20	P11
CN1-17	R0	21	P12
CN1-18	R1	22	P13
CN1-19	R2	23	P14
CN1-20	R3	24	P15
CN1-21	-	-	P16
CN1-22	-	-	P17
CN1-23	-	27	P18
CN1-24	-	28	P19
CN1-25	-	29	P20
CN1-26	-	30	P21
CN1-27	-	31	P22
CN1-28	-	32	P23
CN1-29	PVcc	5	LCD V _{DD}
CN1-30	Vcc	43	Vcc
CN1-31	MODE	44	Vcc
CN1-32	GND	3	GND
CN1-33	GND	4	GND
CN1-34	V _{DD} +12	1	+12 V
CN1-35	ENABKL	40	ENABKL
CN1-36	GND	39	GND

LJ32H028 wiring

LJ32H028		PIA-3386DV CON1	
Pin	Pin name	Pin	Pin name
CN1-1	D1	11	P2
CN1-2	D0	12	P3
CN1-3	D3	9	P0
CN1-4	D2	10	P1
CN1-5	CP2	35	SHF_CLK
CN1-6	GND	3,4	GND
CN1-7	CP1	38	LP
CN1-8	GND	33,34	GND
CN1-9	S	36	FLM
CN1-10	-	-	-
CN1-11	-	-	-
CN1-12	-	-	-
CN1-13	+5 V	43,44	+5 V (V_{DD})
CN1-14	-	-	-
CN1-15	+12 V	1,2	+12 V

Sharp LQ10D42 wiring

(640 x 480 TFT Color)

SHARP LQ10D42		PIA-3386DV CON1	
Pin	Pin name	Pin	Pin name
CN1-1	GND	3,4	GND
CN1-2	CLK	42	SHFCLK
CN1-3	Hsync	38	LP
CN1-4	Vsync	36	FLM
CN1-5	GND	3,4	GND
CN1-6	R0	21	P12
CN1-7	R1	22	P13
CN1-8	R2	23	P14
CN1-9	R3	24	P15
CN1-10	R4	25	P16
CN1-11	R5	26	P17
CN1-12	GND	3,4	GND
CN1-13	G0	15	P6
CN1-14	G1	16	P7
CN1-15	G2	17	P8
CN1-16	G3	18	P9
CN1-17	G4	19	P10
CN1-18	G5	20	P11
CN1-19	GND	3,4	GND
CN1-20	B0	9	P0
CN1-21	B1	10	P1
CN1-22	B2	11	P2
CN1-23	B3	12	P3
CN1-24	B4	13	P4
CN1-25	B5	14	P5
CN1-26	GND	3,4	GND
CN1-27	ENAB	40	M
CN1-28	Vcc	43,44	Vcc +5 V
CN1-29	Vcc	43,44	Vcc +5 V
CN1-30	R/L	-	-
CN1-31	U/D	-	-

SHARP LQ12S31 wiring

(800 x 600 TFT Color)

SHARP LQ12S31		PIA-3386DV CON1	
Pin	Pin name	Pin	Pin name
CN1-1	GND	3	GND
CN1-2	CK	35	SHF_CLK
CN1-3	GND	4	GND
CN1-4	Hsync	38	LP
CN1-5	Vsync	36	FLM
CN1-6	GND	8	GND
CN1-7	GND	8	GND
CN1-8	GND	8	GND
CN1-9	R0	27	P18
CN1-10	R1	28	P19
CN1-11	R2	29	P20
CN1-12	GND	8	GND
CN1-13	R3	30	P21
CN1-14	R4	31	P22
CN1-15	R5	32	
CN1-16	GND	39	GND
CN1-17	GND	39	GND
CN1-18	GND	39	GND
CN1-19	G0	19	P10
CN1-20	G1	20	P11
CN1-21	G2	21	P12
CN1-22	GND	39	GND
CN1-23	G3	22	P13
CN1-24	G4	23	P14
CN1-25	G5	24	P15
CN1-26	GND	41	GND
CN1-27	GND	41	GND
CN1-28	GND	41	GND
CN1-29	B0	11	P2
CN1-30	B1	12	P3
CN1-31	B2	13	P4
CN1-32	GND	41	GND
CN1-33	B3	14	P5
CN1-34	B4	15	P6
CN1-35	B5	16	P7
CN1-36	GND	41	GND
CN1-37	ENAR	37	M
CN1-38	TST	-	-
CN1-49	Vcc	43	+5 V Vcc
CN1-40	Vcc	44	+5 V Vcc
CN1-41	TST		

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AMI BIOS Setup

When the system is powered on, the BIOS will perform diagnostics and initialize system components, including the video system. (This is self-evident when the screen first flicks before the Video Card header is displayed). This is commonly referred as POST (Power-On Self Test). Afterwards, the computer will proceed its final boot-up stage by calling the operating system. Just before that, the user may interrupt to have access to SETUP.

```
AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.16
(C)1996 American Megatrends, Inc. All Rights Reserved

Standard CMOS Setup
Advanced CMOS Setup
Advanced Chipset Setup
Peripheral Setup
Auto-Detect Hard Disks
Change Supervisor Password
Auto Configuration with Optimal Settings
Auto Configuration with Fail Safe Settings
Save Settings and Exit
Exit Without Saving

Standard CMOS setup for changing time, date, hard disk type, etc.
Esc:Exit ↑↓:Sel F2/F3:Color F10:Save & Exit
```

The AMI BIOS is entered by pressing the key after resetting (CTRL-ALT-DEL) or powering up the computer. You can bypass the extended CMOS settings by holding the <INS> key down during boot-up. This is really helpful, especially if you bend the CMOS settings right out of shape and the computer won't boot properly anymore.

The following pages are meant to give you a better insight into the options you have to setup your system. Many options depend on the choice of type of memory, memory speed, peripherals and the programs that you will be running. The effect of many of these settings are related to system performance that can destabilize operation. We urge you to proceed with caution.

Standard CMOS Setup

AMIBIOS SETUP - STANDARD CMOS SETUP										
(C)1996 American Megatrends, Inc. All Rights Reserved										
Date (mm:dd:yyyy) :	Fri, May 14 1999						640 KB			
Time (hh:mm:ss) :	20:37:12						3 MB			
Floppy Drive A	: 1.44M , 3½ in.									
Floppy Drive B	: None									
	Type	Size	Cyln	Head	WPcom	Sec Mode	LBA Blk Mode	PIO Mode	32Bit Mode	
Pri Master :	User	520	1057	16	0	63 On	On	3	Off	
Pri Slave :	Not Installed	0	0	0	0	0 0	0	0	AUTO	
Boot Sector Virus Protection	Disabled									
Month :	Jan - Dec						Esc:Exit	↑↓:sel		
Day :	01 - 31						PgUp/PgDn:Modify			
Year :	1981 - 2099						F2/F3:Color			

Date

The BIOS determines the day of the week from the other date information; this field is for information only.

Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or (key to move to the desired field . Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

Floppy Drive A, B

Select the correct specifications for the diskette drive(s) installed in the computer.

- Not Installed** : No diskette drive installed
- 360K** : 5¼ inch XT-type standard drive
- 1.2M** : 5¼ inch AT-type high-density drive
- 720K** : 3½ inch single-sided drive
- 1.44M** : 3½ inch double-sided drive

Hard Disks

The BIOS supports up to two IDE drives. This section does not show information about other IDE devices, such as a CD-ROM drive, or about other hard drive types, such as SCSI drives.

NOTE : it is recommend that *AUTO* be selected for all drives.

The BIOS can automatically detect the specifications and optimal operating mode of almost all IDE hard drives. When you select type *AUTO* for a hard drive, the BIOS detects its specifications during POST, every time the system boots. If you do not want to select drive type *AUTO*, other methods of selecting the drive type are available:

1. Match the specifications of your installed IDE hard drive(s) with the preprogrammed values for drive types 1 through 46.
2. Select *USER* and enter values into each drive parameter field.
3. Use the IDE HDD *AUTO DETECTION* function in Setup.

Here is a brief explanation of drive specifications:

Type: The BIOS contains a table of predefined drive types. Each defined drive type has a specified number of cylinders, number of heads, write precompensation factor, landing zone, and number of sectors. Drives whose specifications do not accommodate any predefined type are classified as type *USER*.

Size: Disk drive capacity (approximate). Note that this size is usually slightly greater than the size of a formatted disk given by a disk-checking program.

CylIn: Number of cylinders

Head: Number of heads

WPcom: Write Precompensation. Older HDD's have the same number of sectors per track at the innermost tracks as at the outermost tracks. This means that the data density at the innermost tracks is higher and thus the bits are lying closer together. Areas having the same direction tend to float away from each other and areas having opposite direction tend to float towards each other making the data less reliable after some time. To avoid this, starting from the WP cylinder, bits are written on the surface making your data last longer. Starting with this CylNumber until the end of CylNumber s the writing starts earlier on the disk. In modern HDs (all ATBUS and SCSI, Small Computer Systems Interface) this entry is useless.

Sec: Number of sectors

LBA Mode Logical Block Addressing Mode enables support for IDE drives with capacities greater than 528 MB (On/Off)

Block Mode Support IDE drives that use Block Mode. (On/Off)

32Bit Mode Support IDE drives that permit 32-bit accesses. (On/Off)

PIO Mode IDE Programmed I/O mode. PIO programming also works with ATAPI CD-ROM drives. The settings are Auto, 0, 1, 2, 3, 4, or 5. Click on Auto to allow AMIBIOS to automatically find the PIO mode that the IDE drive being configured uses. If you select 0-5 you must make absolutely certain that you are selecting the PIO mode supported by the IDE drive being configured.

BootSector Virus Protection

It is not exactly a virus protection. All it does is whenever your boot sector is accessed for writing, it gives a warning to the screen allowing you to disable the access or to continue. Extremely annoying if you use something like OS/2 Boot Manager that needs to write to it. It is completely useless for SCSI or ESDI (Enhanced Small Device Interface) drives as they use their own BIOS on the controller. Disabled recommended. If you want virus protection, use a TSR (Terminate and Stay Resident) virus detection (Norton, Central Point, etc...). Scan by Macfee is also a good idea. Available on most FTP servers, it is shareware.

Advanced CMOS Setup

AMIBIOS SETUP - ADVANCHED CMOS SETUP		
(C) American Megatrends, Inc. All Rights Reserved		
BootUp Num-Lock	On	Available Options:
Bootup Sequence	C:,A:,CDROM	Off
Floppy Drive Swap	Disabled	▶ On
Floppy Drive Seek	Enabled	
Mouse Support	Enabled	
System Keyboard	Absent	
Primary Display	Absent	
Password Check	Setup	
C000,32k Shadow	Disabled	
C800,32k Shadow	Disabled	
D000,32k Shadow	Disabled	
D800,32k Shadow	Disabled	
E000,32k Shadow	Disabled	
E800,32k Shadow	Disabled	
Esc:Exit ↑↓:Sel PgUP/PgDn:Modify F2/F3:Color		

System Boot Up Num Lock

Specify if you want the Num Lock key to be activated at boot up. MSDOS (starting with version 6) allows a "NUMLOCK=" directive in config.sys, too.

BootUp Sequence

The original IBM PCs loaded the DOS operating system from drive A (floppy disk), so IBM PC-compatible systems are designed to search for an operating system first on drive A, and then on drive C (hard disk). However, modern computers usually load the operating system from the hard drive, and may even load it from a CD-ROM drive.

Floppy Drive Swap

This field is effective only in systems with two floppy drives. Selecting Enabled assigns physical drive B to logical drive A, and physical drive A to logical drive B.

Floppy Drive Seek

When Enabled, the BIOS tests (seeks) floppy drives to determine whether they have 40 or 80 tracks. Only 360-KB floppy drives have 40 tracks; drives with 720 KB, 1.2 MB, and 1.44 MB capacity all have 80 tracks. Because very few modern PCs have 40-track floppy drives, we recommend that you set this field to Disabled to save time.

Mouse Support

This setting is specially for those users who wish to connect a PS/2 mouse. Enabling reserves IRQ 12 for the PS/2 mouse. Disabling releases the IRQ 12 for use by another system component.

System Keyboard

"Present". If "Absent" is selected this option sets the BIOS to pass the keyboard test in the POST, allowing to reset a PC without a keyboard (file server, printer server, etc.), without the BIOS producing a keyboard error.

Primary display

This option specifies the type of display monitor and adapter in the computer. The settings are Mono, CGA40, CGA80, EGA/VGA, or Absent. If you want to use the board without display controller set this value to "Absent". This option sets the BIOS to pass the display controller test in the POST, allowing to boot a PC without a display controller. Even if set to "Absent" the board will still try to initialize a display card if present.

Password Check

If you have set a password, select whether the password is required every time the System boots, or only when you enter the BIOS Setup.

Always	The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
Setup	The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

C000, 32K, Shadow

The story below only applies to ISA based VGA Cards. For modern PCI based display controllers these settings have no effect and might as well be disabled. Memory hidden under the "I/O hole" from 0x0A0000 to 0xFFFFF may be used to "shadow" ROM (Read Only Memory). Doing so, the contents of the ROM are copied into the RAM and the RAM is used instead. Video BIOS is stored in slow EPROM (Erasable Programmable ReadOnly Memory) chips (120 to 150ns of access time). Also, ROM is 8 or 16 bit while RAM 32 bit wide access. With Shadow on, the EPROM content is copied to RAM (60 to 80ns of access time with 32 bit wide access). Therefore performance increases significantly. Only sensible on EGA/VGA systems. C000 has an additional setting called "cached". When "cached is enabled the contents of the named ROM area are written to the same address in system memory (RAM) for faster execution. Additionally, the contents of the RAM area can be read from and written to cache memory.

C800, 32K, Shadow

All addresses (C800 to E800) are for special cards, e.g. network card and SCSI controllers, etc. Enable these only if you have an adapter card with ROM in one of these areas. It is a BAD idea to use shadow RAM for memory areas that aren't really ROM, e.g. network card buffers and other memory mapped devices. This may interfere with the card's operation. To intelligently set these options you need to know exactly which cards use what addresses.

C800, D000, D800, E000, E800

See above

Advanced Chipset Setup

AMIBIOS SETUP - ADVANCHED CHIPSET SETUP		
(C) American Megatrends, Inc. All Rights Reserved		
AT Bus Clock	14.310/2	Available Options:
Slow Refresh	15 μ s	▶ 14.318/2
RAS Precharge time	2.5T	PCLK2/3
CAS Precharge Time Insert Wait	Disable	PCLK2/4
Memory Write Insert Wait	Disable	PCLK2/5
Memory Miss Read Insert Wait	Disable	PCLK2/6
ISA Write cycle end Insert Wait	Disable	PCLK2/8
I/O Recovery	Disable	PCLK2/10
I/O Recovery Period	0 μ s	PCLK2/12
On-Chip I/O Recovery	Disable	
16Bit ISA Insert Wait	Disable	
GPIO [07...00]	IIIIIIIII	
GPIO [15...00]	IIIIIIIII	
Watchdog Function	Enable	
Watchdog Signal	Reset	
Watchdog Timer	64 Sec	
GPCS Function	Enable	Esc:Exit ↑↓:Sel
GPCS0 Command	MEMR/W 8bit	PgUP/PgDn:Modify
GPCS0 Start Address	0C8000 Hex	F2/F3:Color
GPCS0 Size	8 KBYTE	

AT Bus Clock

Gives a division of the CPU clock (or System Clock) so it can reach the ISA - EISA bus clock. An improper setting may cause significant decrease in performance. The settings are in terms of PCLK2/x where x may have values like 2, 3, 4, 5, etc. For 386 processors CLK2 represents half the speed of the CPU. You should try to reach the AT bus speed : 7.15 Mhz. To reach exactly this speed there is a predefined entry that looks like : "14.318/2". You can try other clock settings to increase performance. If you choose a too small divider your system may hang. For a too big divider the performance of ISA cards will decrease. If your ISA cards are fast enough to keep up, it is possible to run the bus at speeds higher than 7.15 Mhz.

Slow Refresh

Causes RAM refresh to happen less often than usual. This increases the performance slightly due to the reduced contention between the CPU and refresh circuitry, but not all DRAM memories necessarily support these reduced refresh rates (in which case you will get parity errors and crashes). Reduced refresh also saves power, a good opportunity for embedded applications

RAS Precharge Time

Technically, this is the duration of the time interval during which the Row Address Strobe signal to a DRAM is held low during normal Read and Write Cycles. This is the minimum interval between completing one read or write and starting another from the same (non-page mode) DRAM. Techniques such as memory interleaving, or use of Page Mode DRAM are often used to avoid this delay. Some chipsets require this parameter in order to set up the memory configuration properly. The RAS Precharge value is typically about the same as the RAM Access (data read/write) time. The latter can be used as an estimate if the actual value is unavailable.

RAS Active Time Insert Wait

Inserts one wait state if enabled in the amount of active time needed for Row Address Strobe during refresh. Disabling this option increases performance.

CAS Precharge Time Insert Wait

Inserts one wait state. Determines the number of CPU clock cycles allocated for the CAS signal to accumulate its charge before EDO DRAM is allowed to precharge. If insufficient time is allowed, refresh may be incomplete and data lost.

Memory Write Insert Wait

Wait states is for RAM which aren't fast enough for the computer. On a 486, 1 or more wait states are often required for RAM with 80ns or higher access time. And, depending on the processor and mother board, also for lower than 80ns access time. The less wait states, the better. If wait states are too low, a parity error will occur. For 386 or 486 nonburst memory access cycle takes 2 clock ticks. A *rough* indication of RAM speed necessary for 0 wait states is $2000/\text{Clock}[\text{MHz}]/10$ [ns]. For a 40Mhz processor, this would give 50ns of access time required. The number of wait states necessary is *approximately* $(\text{RamSpeed}[\text{ns}] + 10) * \text{Clock}[\text{MHz}] / 1000$. For 70ns RAM and a 33Mhz processor (very standard configuration), this would give roughly 1 wait state. But this really is dependent on chip set, mother board and cache design, CPU type and whether we talk about reads or writes. Take these formulas with a large grain of salt. You can find out the access time of your RAM chips by looking at their product numbers. Mostly at the end there is a 70, 80, 90, or even 60. If 10 stands there, it means 100 ns. Some RAM chips also have an explicitly written speed in ns. The RAM you buy these days mostly have 70ns or 60ns.

Memory Miss Insert Wait

Same as above. Select Enabled if the installed DRAM requires additional wait states. Do not change from the default setting unless you are experiencing memory errors.

ISA Write cycle end Insert Wait

If you have add-on RAM in an ISA expansion slot, select Enabled to allow additional time for the slower throughput of the ISA bus.

I/O Recovery

When enabled, allows you to insert wait states (see "I/O Recovery Period")

I/O Recovery Period

When enabled, more I/O wait states are inserted. A transfer from IDE hard-drive to memory happens without any handshaking, meaning the data has to be present (in the cache of the hard disk) when the CPU wants to read them from an I/O Port. This is called PIO (Programmed I/O) and works with a REP INSW assembler instruction. Now I/O Recovery Time enabled adds some wait states to this instruction. When disabled, the harddrive is a lot faster. Note that there is a connection between I/O Recovery Time and AT BUS Clock Selection. For example, if the AT BUS Clock is set to 8 MHZ and you have a normal hard disk, I/O Recovery Time can be turned off, resulting in a higher transfer rate from hard disk.

On-Chip I/O Recovery

Select Enabled to allow extra preparation time between I/O cycles controlled by the M6117D chip.

16Bit ISA Insert Wait

Your system quite possibly has much higher performance than some of your input/output (I/O) devices. This means that unless the system is instructed to allow more time, more wait states, for devices to respond, it might think the device has malfunctioned and stop its request for I/O. If all your I/O devices are capable, then disabling this setting could result in greater throughput. Otherwise, data could be lost.

Watchdog Function

Disable enable the time-out function of the M6117D watchdog timer. The watchdog timer can either be setup in the BIOS or can be configured by writing directly to the watchdog registers. If the watchdog control by software is preferred than disable the watchdog in the BIOS setup !

Watchdog Signal

This defines the action that will be undertaken once the watchdog has timed out. The action can be either RESET, NMI or IRQ 3/4/5/6/7/9/10/11/12/14/15

Watchdog Timer

Choose the time-out period 1/2/4/8/16/32/64/128/256/512 Seconds. The watchdog timer is a down timer. If set to 16 seconds it will count down to 0 and invoke a RESET, NMI or IRQ. If during the countdown period the watchdog receives a reset signal it aborts the countdown and starts a new countdown sequence from 16.

GPCS Function

Enable or Disable the DiskOnChip function

GPCS0 Command

for DiskOnChip always MEMR/W 8bit

GPCS0 Start Address

Choose the DiskOnChip base address.
Valid range between C8000h DE000h

GPCS0 Size

for DiskOnChip always 8 KBYTE

Peripheral Setup

AMIBIOS SETUP - PERIPHERAL SETUP		
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Onboard IDE	Primary	Available Options:
Hard disk Delay	Disabled	Disabled
Onboard FDC	Enabled	▶ Primary
Onboard Serial Port 1	3F8h	Secondary
Serial Port1 Mode	Normal	
Serial Port1 Duplex	Full	
Onboard Serial Port 2	2F8h	
Serial Port2 Mode	Normal	
Serial Port2 Duplex	Full	
Onboard Parallel Port	278h	
Parallel Port Mode	Disable	
EPP Version	N/A	
Parallel Port DMA Channel	N/A	
Parallel Port IRQ	7	
		Esc:Exit ↑↓:sel PgUP/PgDn:Modify F2/F3:Color

Onboard IDE

This option specifies the channel used by the IDE controller on the motherboard. Primary or Secondary.

Hard disk Delay

Delay for a connected SCSI HDD (Secs). The length of time in seconds the BIOS will wait for a SCSI hard disk to be ready for operation. If the hard drive is not ready, the SCSI BIOS might not detect the hard drive correctly. The range is from 0-15 seconds.

Onboard FDC

Enable/disable FDD Controller

Onboard Serial Port1 (or 2) Disable or enable with I/O address: 3F8h for port 1, and 2F8h for port 2.

Serial Port1 (or 2) Mode

Normal for standard serial port operation, SIR for Serial Infrared operation, ASKIR for Amplitude Shift Keyed IR interface.

Serial Port1 (or 2) Duplex

A link can be either half or full duplex. Full duplex allows a port to transmit without effecting its receiver's functioning. Half duplex is similar to full duplex with the exception that the transmitter's operation causes the receiver to be shut-off.

Onboard Parallel Port

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications. The settings are 378h, 278h, or Disabled.

Norma	The normal parallel port mode is used.
Bi-Dir	Supports bidirectional transfers on the parallel port.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5 Mbs. ECP provides symmetric bidirectional communications.

Parallel Port DMA

This option is only available if the setting for the Parallel Port Mode option is ECP. The settings are Disabled, DMA CH (channel) 0, DMA CH 1, or DMA CH 3. The default setting is Disabled.

Auto-Detect Hard Disks

Brings up the "Standard CMOS Setup" screen and automatically scans the IDE devices to detect any connected harddisks.

Change Supervisor Password

Configure a Boot or Setup password.

Auto Configuration with Optima Settings

These settings provide the best performance characteristics.

Auto Configuration with Fail Safe Settings

These settings are more likely to configure a workable computer when something is wrong. If you cannot boot the computer successfully, select the Fail-Safe Setup options and try to diagnose the problem after the computer boots. These settings do not provide optimal performance.

POST Error Codes

During the POST routines, which are performed each time the system is powered on, errors may occur. Non-fatal errors are those which, in most cases, allow the system to continue the boot process. Error messages would normally appear on the screen. Fatal errors are those which will not allow the system to continue the boot procedure. If a fatal error occurs, you should consult your system manufacturer or dealer for possible solutions or repairs. These fatal errors are usually communicated through a series of audible beeps. All errors listed, with the exception of 8 beeps, are fatal errors. All errors found by the BIOS will be forwarded to the I/O port 80h.

Audible (beep) Error Messages

- 1 beep DRAM refresh failure. The memory refresh circuitry on the motherboard is faulty.
- 2 beeps Parity Circuit failure. A parity error was detected in the base memory (first 64k Block) of the system.
- 3 beeps Base 64K RAM failure. A memory failure occurred within the first 64k of memory.
- 4 beeps System Timer failure. Timer #1 on the system board has failed to function properly.
- 5 beeps Processor failure. The CPU on the system board has generated an error.
- 6 beeps Keyboard Controller 8042-Gate A20 error. The keyboard controller (8042) contains the gate A20 switch which allows the computer to operate in virtual mode. This error message means that the BIOS is not able to switch the CPU into protected mode.
- 7 beeps Virtual Mode (processor) Exception error. The CPU on the motherboard has generated an Interrupt Failure exception interrupt.
- 8 beeps Display Memory R/W Test failure. The system video adapter is either missing or Read/Write Error its memory is faulty. This is not a fatal error.
- 9 beeps ROM-BIOS Checksum failure. The ROM checksum value does not match the value encoded in the BIOS. This is good indication that the BIOS ROMs went bad.
- 10 beeps CMOS Shutdown Register. The shutdown register for the CMOS memory Read/Write Error has failed.
- 11 beeps Cache Error / External Cache Bad. The external cache is faulty.

Other AMI BIOS POST Codes

- 2 short beeps POST failed. This is caused by a failure of one of the hardware testing procedures.
- 1 long & 2 short beeps Video failure. This is caused by one of two possible hardware faults. 1) Video BIOS ROM failure, checksum error encountered. 2) The video adapter installed has a horizontal retrace failure.
- 1 long & 3 short beeps: Video failure. This is caused by one of three possible hardware problems. 1) The video DAC has failed. 2) the monitor detection process has failed. 3) The video RAM has failed.
- 1 long beep: POST successful. This indicates that all hardware tests were completed without encountering errors.

Troubleshooting

1 beep, 2 beeps, or 3 beeps

try reseating the memory first. If the error still occurs, replace the memory with known good chips.

4 beeps, 6 beeps, 5 beeps, 7 beeps, or 10 beeps

the system board must be sent in for repair.

8 beeps

indicates a memory error on the video adapter. Replace the video card or the memory on the video card.

9 beeps

indicates faulty BIOS chip(s). It is not likely that this error can be corrected by reseating the chips. Consult the motherboard supplier for replacement part(s).

No beeps, No boot

If no beeps are heard and no display is on the screen, The first thing to check is the power supply. Connect a LED to the POWER LED connection on the motherboard. If this LED lights and the drive(s) spin up then the power supply will usually be good.

Next, inspect the motherboard for loose components. A loose or missing CPU, BIOS chip, Crystal Oscillator, or Chipset chip will cause the motherboard not to function.

Next, eliminate the possibility of interference by a bad or improperly set up I/O card by removing all card except the video adapter. The system should at least power up and wait for a drive time-out. Insert the cards back into the system one at a time until the problem happens again. When the system does nothing, the problem will be with the last expansion card that was put in.

If the above suggestions fail to cause any change in the disfunction of the system, the motherboard must be returned for repair.

Visible (screen) Error Messages

8042 Gate A20 Error :

Gate A20 on the keyboard controller (8042) is not working.

Address Line Short! :

Error in the address decoding circuitry.

Cache Memory Bad, Do Not Enable Cache! :

Cache memory is defective.

CH2 Timer Error :

There is an error in timer 2. Several systems have two timers.

CMOS Battery State Low :

The battery power is getting low. It would be a good idea to replace the battery.

CMOS Checksum Failure :

After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value.

CMOS System Options Not Set :

The values stored in CMOS RAM are either corrupt or nonexistent.

CMOS Display Type Mismatch :

The video type in CMOS RAM is not the one detected by the BIOS.

CMOS Memory Size Mismatch :

The physical amount of memory on the motherboard is different than the amount in CMOS RAM.

CMOS Time and Date Not Set :

Self evident.

Diskette Boot Failure :

The boot disk in floppy drive A: is corrupt (virus?). Is an operating system present?

Display Switch Not Proper :

A video switch on the motherboard must be set to either color or monochrome.

DMA Error :

Error in the DMA controller.

DMA number 1 Error :

Error in the first DMA channel.

DMA number 2 Error :

Error in the second DMA channel.

FDD Controller Failure :

The BIOS cannot communicate with the floppy disk drive controller.

HDD Controller Failure :

The BIOS cannot communicate with the hard disk drive controller.

INTR number 1 Error :

Interrupt channel 1 failed POST.

INTR number 2 Error :

Interrupt channel 2 failed POST.

Keyboard Error :

There is a timing problem with the keyboard.

KB/Interface Error :

There is an error in the keyboard connector.

Parity Error ???? :

Parity error in system memory at an unknown address.

Memory Parity Error at xxxxx :

Memory failed at the xxxxx address.

I/O Card Parity Error at xxxxx :

An expansion card failed at the xxxxx address.

DMA Bus Timeout :

A device has used the bus signal for more than allocated time (around 8 microseconds).

POST Card Codes

The following codes are not displayed on the screen. They can only be viewed on the LED display of a so called POST card. The codes are listened in the same order as the according functions are executed at PC startup. If you have access to a POST Card reader, you can watch the system perform each test by the value that's displayed. If the system hangs (if there's a problem) the last value displayed will give you a good idea where and what went wrong, or what's bad on the system board.

CHECK DESCRIPTION OF CHECK

- | | |
|----|--|
| 01 | Processor register test about to start, and NMI to be disabled. |
| 02 | NMI is Disabled. Power on delay starting. |
| 03 | Power on delay complete. Any initialization before keyboard BAT is in progress. |
| 04 | Any initialization before keyboard BAT is complete. Reading keyboard SYS bit, to check soft reset/ power-on. |
| 05 | Soft reset/ power-on determined. Going to enable ROM. i.e. disable shadow RAM/Cache if any. |
| 06 | ROM is enabled. Calculating ROM BIOS checksum, and waiting for KB controller input buffer to be free. |
| 07 | ROM BIOS checksum passed, KB controller I/B free. Going to issue the BAT command to keyboard controller. |
| 08 | BAT command to keyboard controller is issued. Going to verify the BAT command. |
| 09 | Keyboard controller BAT result verified. Keyboard command byte to be written next. |
| 0A | Keyboard command byte code is issued. Going to write command byte data. |
| 0B | Keyboard controller command byte is written. Going to issue Pin-23,24 blocking/unblocking command. |
| 0C | Pin-23,24 of keyboard controller is blocked/ unblocked. NOP command of keyboard controller to be issued next. |
| 0D | NOP command processing is done. CMOS shutdown register test to be done next. |
| 0E | CMOS shutdown register R/W test passed. Going to calculate CMOS checksum, and update DIAG byte. |
| 0F | CMOS checksum calculation is done, DIAG byte written. CMOS init. to begin (If "INIT CMOS IN EVERY BOOT IS SET"). |
| 10 | CMOS initialization done (if any). CMOS status register about to init for Date and Time. |
| 11 | CMOS Status register initialized. Going to disable DMA and Interrupt controllers. |
| 12 | DMA controller #1,#2, interrupt controller #1,#2 disabled. About to disable Video display and init port-B. |

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- 13 Video display is disabled and port-B is initialized. Chipset init/ auto memory detection about to begin.
- 14 Chipset initialization/ auto memory detection over. 8254 timer test about to start.
- 15 CH-2 timer test halfway. 8254 CH-2 timer test to be complete.
- 16 Ch-2 timer test over. 8254 CH-1 timer test to be complete.
- 17 CH-1 timer test over. 8254 CH-0 timer test to be complete.
- 18 CH-0 timer test over. About to start memory refresh.
- 19 Memory Refresh started. Memory Refresh test to be done next.
- 1A Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time.
- 1B Memory Refresh period 30 micro second test complete. Base 64K memory test about to start.
- 20 Base 64k memory test started. Address line test to be done next.
- 21 Address line test passed. Going to do toggle parity.
- 22 Toggle parity over. Going for sequential data R/W test.
- 23 Base 64k sequential data R/W test passed. Any setup before Interrupt vector init about to start.
- 24 Setup required before vector initialization complete. Interrupt vector initialization about to begin.
- 25 Interrupt vector initialization done. Going to read I/O port of 8042 for turbo switch (if any).
- 26 I/O port of 8042 is read. Going to initialize global data for turbo switch.
- 27 Global data initialization is over. Any initialization after interrupt vector to be done next.
- 28 Initialization after interrupt vector is complete. Going for monochrome mode setting.
- 29 Monochrome mode setting is done. Going for Color mode setting.
- 2A Color mode setting is done. About to go for toggle parity before optional rom test.
- 2B Toggle parity over. About to give control for any setup required before optional video ROM check.
- 2C Processing before video ROM control is done. About to look for optional video ROM and give control.
- 2D Optional video ROM control is done. About to give control to do any processing after video ROM returns control.
- 2E Return from processing after the video ROM control. If EGA/VGA not found then do display memory R/W test.
- 2F EGA/VGA not found. Display memory R/W test about to begin.
- 30 Display memory R/W test passed. About to look for the retrace checking.
- 31 Display memory R/W test or retrace checking failed. About to do alternate Display memory R/W test.

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- 32 Alternate Display memory R/W test passed. About to look for the alternate display retrace checking.
- 33 Video display checking over. Verification of display type with switch setting and actual card to begin.
- 34 Verification of display adapter done. Display mode to be set next.
- 35 Display mode set complete. BIOS ROM data area about to be checked.
- 36 BIOS ROM data area check over. Going to set cursor for power on message.
- 37 Cursor setting for power on message id complete. Going to display the power on message.
- 38 Power on message display complete. Going to read new cursor position.
- 39 New cursor position read and saved. Going to display the reference string.
- 3A Reference string display is over. Going to display the Hit <ESC> message.
- 3B Hit <ESC> message displayed. Virtual mode memory test about to start.
- 40 Preperation for virtual mode test started. Going to verify from video memory.
- 41 Returned after verifying from display memory. Going to prepare the descriptor tables.
- 42 Descriptor tables prepared. Going to enter in virtual mode for memory test.
- 43 Entered in the virtual mode. Going to enable interrupts for diagnostics mode.
- 44 Interrupts enabled (if diagnostics switch is on). Going to initialize data to check memory wrap around at 0:0.
- 45 Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
- 46 Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
- 47 Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
- 48 Patterns written in base memory. Going to find out amount of memory below 1M memory.
- 49 Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
- 4A Amount of memory above 1M found and verified. Going for BIOS ROM data area check.
- 4B BIOS ROM data area check over. Going to check <ESC> and to clear memory below 1M for soft reset.
- 4C Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.

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- 4D Memory above 1M cleared. (SOFT RESET) Going to save the memory size.
- 4E Memory test started. (NO SOFT RESET) About to display the first 64k memory test.
- 4F Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
- 50 Memory test below 1M complete. Going to adjust memory size for relocation/ shadow.
- 51 Memory size adjusted due to relocation/ shadow. Memory test above 1M to follow.
- 52 Memory test above 1M complete. Going to prepare to go back to real mode.
- 53 CPU registers are saved including memory size. Going to enter in real mode.
- 54 Shutdown successful, CPU in real mode. Going to restore registers saved during preparation for shutdown.
- 55 Registers restored. Going to disable gate A20 address line.
- 56 A20 address line disable successful. BIOS ROM data area about to be checked.
- 57 BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
- 58 BIOS ROM data area check over. Going to clear Hit <ESC> message.
- 59 Hit <ESC> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
- 60 DMA page register test passed. About to verify from display memory.
- 61 Display memory verification over. About to go for DMA #1 base register test.
- 62 DMA #1 base register test passed. About to go for DMA #2 base register test.
- 63 DMA #2 base register test passed. About to go for BIOS ROM data area check.
- 64 BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
- 65 BIOS ROM data area check over. About to program DMA unit 1 and 2.
- 66 DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
- 67 8259 initialization over. About to start keyboard test.
- 80 Keyboard test started. clearing output buffer, checking for stuck key, About to issue keyboard reset command.
- 81 Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.

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- 82 Keyboard controller interface test over. About to write command byte and init circular buffer.
- 83 Command byte written, Global data init done. About to check for lock-key.
- 84 Lock-key checking over. About to check for memory size mismatch with cmos.
- 85 Memory size check done. About to display soft error and check for password or bypass setup.
- 86 Password checked. About to do programming before setup.
- 87 Programming before setup complete. Going to cmos setup program.
- 88 Returned from cmos setup program and screen is cleared. About to do programming after setup.
- 89 Programming after setup complete. Going to display power on screen message.
- 8A First screen message displayed. About to display <WAIT...>message
- 8B <WAIT...> message displayed. About to do Main and Video BIOS shadow.
- 8C Main and Video BIOS shadow successful. Setup options programming after cmos setup about to start.
- 8D Setup options are programmed, mouse check and init to be done next.
- 8E Mouse check and initialization complete. Going for hard disk, floppy reset.
- 8F Floppy check returns that floppy is to be initialized. Floppy setup to follow.
- 90 Floppy setup is over. Test for hard disk presence to be done.
- 91 Hard disk presence test over. Hard disk setup to follow.
- 92 Hard disk setup complete. About to go for BIOS ROM data area check.
- 93 BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
- 94 BIOS ROM data area check over. Going to set base and extended memory size.
- 95 Memory size adjusted due to mouse support, hdisk type-47. Going to verify from display memory.
- 96 Returned after verifying from display memory. Going to do any init before C800 optional ROM control
- 97 Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
- 98 Optional ROM control is done. About to give control to do any required precessing after optional ROM returns control.
- 99 Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.

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- 9A Return after setting timer and printer base address. Going to set the RS-232 base address.
 - 9B Returned after RS-232 base address. Going to do any initialization before Coprocessor test
 - 9C Required initialization before coprocessor is over. Going to initialize the coprocessor next.
 - 9D Coprocessor initialized. Going to do any initialization after Coprocessor test.
 - 9E Initialization after coprocessor test is complete. Going to check extd keyboard, keyboard ID and num-lock.
 - 9F Extd keyboard check is done, ID flag set. num-lock on/off. Keyboard ID command to be issued.
 - A0 Keyboard ID command issued. Keyboard ID flag to be reset.
 - A1 Keyboard ID flag reset. Cache memory test to follow.
 - A2 Cache memory test over. Going to display any soft errors.
 - A3 Soft error display complete. Going to set the keyboard typematic rate.
 - A4 Keyboard typematic rate set. Going to program memory wait states.
 - A5 Memory wait states programming over. Screen to be cleared next.
 - A6 Screen cleared. Going to enable parity and NMI.
 - A7 NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
 - A8 Initialization before E000 ROM control over. E000 ROM to get control next.
 - A9 Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
 - AA Initialization after E000 optional ROM control is over. Going to display the system configuration.
 - 00 System configuration is displayed. Going to give control to INT 19h boot loader.

Howto : Flash the BIOS

What do you need ?

To flash your BIOS you'll need

- 1) a xxxxx.rom file that is a file image of the new BIOS
- 2) FLASH634.EXE a utility that can write the data-file into the BIOS chip.

The procedure

Create a new, clean DOS (format under Win95/Win98 etc is acceptable as long as the disk can boot) bootable floppy with "format a: /s".

Copy flash utility and the BIOS image file to this disk.

Make sure you have a complete and full back up of your data. Also make sure you have copied all of the CMOS settings down prior to making any BIOS changes.

Boot MS-DOS from the floppy and run the flash writer with the image file name as argument eg:

```
FLASH634 xxxxxx.ROM
```

After the writer is completed, turn off the system power and turn back on to boot

Enter the CMOS setup (either press F1 or the DEL key).

Set everything to the defaults and check your system.

What if things go wrong

If you use the wrong Flash BIOS or if the writing process gets interrupted, there is a fat chance that your computer won't boot anymore. Then please contact your local dealer to fix your problem.

Warranty

This product is warranted to be in good working order for a period of one year from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.

